

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1011	703/14.ccls.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 14:47

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	2	"6573744".pn.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:12
2	BRS	L2	92	tsai-r.in.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:15
3	BRS	L3	5175	(bias same dependence)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:32
4	BRS	L4	242	(bias adj dependence)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:33
5	BRS	L5	11	(bias adj dependence) same temperature same process	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:35

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	90	(semiconductor) and (bias adj dependence) and (temperature) and process	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:36
7	BRS	L7	3	(semiconductor) and (bias adj dependence) and (temperature) and process and (lay adj out)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:47
8	BRS	L8	45194	(semiconductor) same subsequent	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:47
9	BRS	L9	5	((semiconductor) same subsequent) and (s-parameter)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:48
10	BRS	L10	1	((semiconductor) same subsequent) and (s-parameter) and SEM	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:48

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	3	((semiconductor) same subsequent) and (s-parameter) and (semiconductor same characteristics)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:48
12	BRS	L12	3	((semiconductor) same subsequent) and (s-parameter) and (semiconductor same characteristics) and fabrication	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:51
13	BRS	L13	1	((semiconductor) same subsequent) and (equivalent adj model) and (semiconductor same characteristics) and fabrication	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:51
14	BRS	L14	2	((semiconductor) same subsequent) and (equivalent adj model) and fabrication	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:51
15	BRS	L15	85	((semiconductor) same subsequent) and (equivalent same model) and fabrication	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/06/29 09:52

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	4	((semiconductor) same subsequent) and (equivalent same model same fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:55
17	BRS	L17	163	(equivalent same model same fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:55
18	BRS	L18	1	((equivalent adj model) same fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:55
19	BRS	L19	100	((equivalent adj model) and fabrication)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:56
20	BRS	L20	16	((equivalent adj model) same semiconductor)	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:56

	Type	L #	Hits	Search Text	DBs	Time Stamp
21	BRS	L21	0	((equivalent adj model) same semiconductor) and subsequent	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 09:57
22	BRS	L22	5	((equivalent adj model) same semiconductor) and subsequent	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 10:29
23	BRS	L23	2	"5878053".pn.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 10:31
24	BRS	L24	1	"5878053".pn. and average	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 10:42
25	BRS	L25	1	"5878053".pn. and characteristics	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 11:03

	Type	L #	Hits	Search Text	DBs	Time Stamp
26	BRS	L26	1	"5878053".pn. and sample	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/06/29 11:03



bias temperature process scaling layout SEM

[Advanced Scholar Search](#)

[Scholar Preferences](#)

[Scholar Help](#)

Scholar Results 1 - 10 of about 839 for **bias temperature process scaling layout SEM "semiconductor"**. (1)

[An edge-defined nano-lithography technique suitable for low thermal budget process and 3-D stackable ...](#)

J Nasrullah, JB Burr, GL Tyler - Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE ... , 2003 - ieeexplore.ieee.org

... 400mT, 1400W RF power, and electrode **bias** of — 530V ... Their **process** used high-temperature oxide for the etch ... such as this edge-defined **process** potentially offer ...

[Cited by 1 - Web Search](#)

[ESD Scalability of LDMOS Devices for Self-Protected Output Drivers](#)

Y Chung, H Xu, R Ida, WG Min, B Baird - Power **Semiconductor** Devices and ICs, 2005. Proceedings. ... , 2005 - ieeexplore.ieee.org

... grounded-gate (gg) condition, junction **temperature** profile within ... 1000u, as a function of the gate **bias**. ... geometries under snapback breakdown **process** has been ...

[Web Search](#)

[RHEA \(resist-hardened etch and anodization\) **process** for fine-geometry Josephson junction fabrication - group of 2 »](#)

LPS Lee, ER Arambula, G Hanaya, C Dang, R Sandell, ... - Magnetics, IEEE Transactions on, 1991 - ieeexplore.ieee.org

... CD with a constant CD **bias** improves the ... and J. Pacansky, "High Temperature Flow Resistance ... Jiltie, "Selective niobium anodization **process** for fabricating ...

[Cited by 8 - Web Search](#)

[Mechanical Stress Induced MOSFET Punch-through And **Process** Optimization For Deep Submicron TEOS-O/ ...](#)

K Ishimaru, F Matsuoka, M Takahashi, M Nishigohri, ... - VLSI Technology, 1997. Digest of Technical Papers., 1997 ... , 1997 - ieeexplore.ieee.org

... Optimized high **temperature** annealing achieved defect free characteristics and ... **Process** integration for future STI devices should take ... 6 8 1 0 Reverse Bias (V) (b ...

[Cited by 7 - Web Search - BL Direct](#)

[An ultra dense trench-gated power MOSFET technology using a self-aligned **process**](#)

J Zeng, G Dolny, C Kocon, R Stokes, N Kraft, L ... - Power **Semiconductor** Devices and ICs, 2001. ISPSD'01. ... , 2001 - ieeexplore.ieee.org

... The **process** and physical models, as well as ... **temperature** gate **bias** (HTGB), humidity **bias**, autoclave, **temperature** ... level at the zero **temperature**-coefficient point ...

[Cited by 6 - Web Search](#)

[Sensors and the Influence of **Process** Parameters and Thin Films - group of 2 »](#)

HR Krauss - ADVANCES IN SOLID STATE PHYSICS-PERGAMON PRESS THEN VIEWEG-, 2002 - Springer

... 6). After **process** related **temperature** treatment voids are formed ... polysilicon layer,

V is the **bias** voltage across ... scale regions and to get **process** tolerances by ...

[Web Search - BL Direct](#)

[MEMS Packaging on a Budget \(Fiscal and Thermal\)](#)

MB Cohn, R Roehnelt, JH Xu, A Shtenberg, S Cheung ... - ieeexplore.ieee.org

... up to 5 RF interconnects, and 4 **bias** connections ... can be performed within the back-end **temperature** range of ... values are on par with those of a monolithic **process**. ...

[Cited by 5 - Web Search](#)

No-Fault Assurance: Linking Fast Process CAD and EDA - group of 2 »

A Neureuther, F Gennari - Proc. SPIE, 2002 - eecs.berkeley.edu

... Bias ... The accuracy of this **temperature** cooling estimate is obviously rather ... be used to communicate among circuit designers, mask makers and **process** technologists ...Cited by 6 - [View as HTML](#) - [Web Search](#)Vertical sige-base bipolar transistors on cmos-compatible soi substrate

J Cai, M Kumar, M Steigerwalt, H Ho, K Schonenberg ... - Bipolar/BiCMOS Circuits and Technology Meeting, 2003. ..., 2003 - ieeexplore.ieee.org

... by varying collector doping, **layout** and SQL substrate **bias**. ... that of a bulk SiGe bipolar **process** [6]. An ... stack, using the UHV/CVD Low-Temperature-Epitaxy (LTE ...Cited by 9 - [View as HTML](#) - [Web Search](#)Fabricating 90 nm Devices by 2004

S Equipment - kla-tencor.com

... replicate the customers' design rules and **bias**," said KLA's ... In the S/D, the **process** calls for ... preferably with instantaneous time-at-**temperature** (spike anneal ...[View as HTML](#) - [Web Search](#)

Gooooooooogle ►

Result Page: 1 2 3 4 5 6 7 8 9 10 [Next](#) [Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2006 Google

[Advanced Scholar Search](#)
[Scholar Preferences](#)
[Scholar Help](#)**Scholar**Results 1 - 3 of 3 for S-parameter "Roger Tsai". (0.11 seconds)

Tip: Try removing quotes from your search to get more results.

2 ndGeneration Device Modeling for MMIC Design & Manufacturability - group of 9 »[All articles](#) [Recent articles](#)

R Tsai, M Nishimoto, W Akiyama, J Chang, D Ko, A ... - [ssl6.pair.com](#)
... CA 90278 Tel: (310) 812-8254, Fax: (310) 813-0418, Email: roger.tsai@trw.com ... If we
trusted our **S- parameter** measurements up to only 50 GHz, customers doing V ...
[View as HTML](#) - [Web Search](#)

Through-the-lens camera control - group of 12 »

M Gleicher, A Witkin - ACM SIGGRAPH Computer Graphics, 1992 - [portal.acm.org](#)
... Because the error norm of equation 6 is the Euclidean distance in the camera's
parameter space, rather than being intrinsic to the world-space camera motion ...
[Cited by 130](#) - [Web Search](#) - [BL Direct](#)

Through-the-Lens Camera Control - group of 2 »

PA Pittsburgh - [cs.princeton.edu](#)
... Because the error norm of equation 6 is the Euclidean distance in the camera's
parameter space, rather than being intrinsic to the world-space camera motion ...
[View as HTML](#) - [Web Search](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2006 Google